REMARKS

In the August 11, 2004 Office Action, all of the pending claims 1-15 were rejected. Claim 5 was rejected in view of U.S. Pat. No. 6,205,537 ("Albonesi"), presumably under 35 U.S.C. §102(e). Further, it appears that the Examiner has continued to reject claims 1-4 and 6-15 under 35 U.S.C. §103(a) as unpatentable over Albonesi, in view of U.S. Pat. No. 4,907,148 ("Morton").

Claim 5 has been amended to recite that a plurality of control signals are used to enable a selected subset of cells in the MxN array. Support for this amendment can be found at page 4 lines 6-11, for example.

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Applicants traverse the rejection of claim 5.

Albonesi discloses a dynamically reconfigurable microprocessor having multiple processor elements that are arranged in a linear configuration, and each element is controlled using a single control signal (see FIG. 4). In contrast, amended claim 5 is directed to power saving in an M row by N column processor. Claim 5 recites the step of "masking an MxN array of processor cells using a plurality of control signals to enable a subset of cells." Albonesi does not disclose an MxN processor array or the masking of such an array using a plurality of control signals to enable active cells and to disable inactive cells such that they do not consume power.

For at least the above reasons, Albonesi does not anticipate the invention of claim 5 and withdrawal of the §102(e) rejection of claim 5 is respectfully requested.

Applicants traverse the rejection Claims 1-4 and 6-15 over Albonesi in view of Morton.

Regarding claim 1, the combination of Albonesi and Morton does not teach or suggest the step of "gating the row mask signal and column mask signal with a clock signal of each cell" as recited in claim 1. The Examiner has identified in Fig. 4, the elements 40 (Control Register), "Processor Active", and "CLK." However, it is respectfully submitted that, as indicated by col. 4, lines 12-16, the "Processor Active" signal is in reality an output of AND gate 41, which in turn is determined by the data being shifted through Control Register 40 using, among other signals, the CLK signal. Thus, it is respectfully submitted that even if Albonesi were combined with Morton as asserted by the Examiner, at the very least, the gating step of claim 1 would not be met. Further, Morton teaches away from this limitation as evidenced by the array processor cell

shown in Morton's FIG. 4, which continues to receive and operate on at least one clock signal regardless of its "active" or "inactive" status. Also as mentioned above, Albonesi does not disclose an MxN processor array. Nor does Albonesi disclose the use of row and column mask signals. Consequently, Applicants submit that it would not have been obvious to use the clock signal of Albonesi to gate row and column mask signals that were not even contemplated by Albonesi.

Furthermore, one skilled in the art would not be motivated to combine Albonesi and Morton. For example, the processor of Morton is intended to overcome prior art processors where "only a single control bit per cell" is provided (Column 2, Lines 20-22). Albonesi, however, discloses such a processor architecture, i.e., one where each element is enabled/disabled with one control signal (see FIG. 4 of Albonesi). Accordingly, Morton teaches away from the control signal methodology of Albonesi and one skilled in the art would not be motivated to make the proposed combination.

For at least the above reasons, claim 1, and claims 2-4, which ultimately depend from claim 1, are patentable over Albonesi in view of Morton, and the Examiner's indication to that end is respectfully requested.

Regarding claim 6, it is respectfully submitted that the combination of Albonesi and Morton does not teach or suggest "a clock circuit, connected to supply each cell with a clock signal, each clock signal being gated with the row mask signal and column mask signal" as recited in claim 6. As indicated for control register 40 in Fig. 4 by col. 7, lines 51-55, of Morton, the clock signal participates in the entering of data into control register 40 from the right or left. See, col. 7, lines 55-58. Thus, even if Albonesi and Morton were combined as asserted by the Examiner, the combination cannot be said to operate as in claim 6 where a clock signal that is supplied to each cell, is gated with the row mask signal and column mask signal.

For at least the above reasons, claim 6, and claims 7-10, which ultimately depend from claim 6, are patentable over Albonesi in view of Morton, and the Examiner's indication to that end is respectfully requested.

Regarding claim 11, the combination of Albonesi and Morton does not teach or suggest each and every claim limitation. For the reasons discussed above in connection with claim 1, the combination does not teach or suggest "a clock for providing a clock signal, the clock signal being gated with the mask signal" as recited in claim 11. In addition, for the reasons discussed

above in connection with claim 1, one skilled in the art would not be motivated to combine Albonesi and Morton.

For at least the above reasons, claim 11, and claims 12-15, which variously depend from claim 11, are not unpatentable over Albonesi in view of Morton. Therefore, Applicants request the withdrawal of the §103(a) rejection of those claims.

The Commissioner is hereby authorized to charge any fees that may be associated with this communication to Deposit Account No. 07-1896.

Respectfully submitted,

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